Amendments to the Claims

The listing of claims will replace all prior versions, listings, of claims in the application.

Listing of Claims

Claims 1-4 (Canceled)

5. (Previously Amended) An enhanced one-wire bus for the half duplex transmission of serial data between a master and a slave comprising:

a translator having a primary interface, a secondary interface, and data storage;

a primary one wire bus in electrical communication with said primary interface and with the master;

a secondary one wire bus in electrical communication with said secondary interface and the slave device,

wherein,

when said translator is in a first operational mode, said primary interface is in electrical communication with said secondary interface such that serial data on said primary one wire bus is communicated to said secondary one wire bus,

when said translator is in a second operational mode, said primary interface is in electrical communication with said secondary interface such that serial data on said secondary one wire bus is communicated to said primary one wire bus, and

when said translator is in a third operational mode, said primary interface is in electrical communication with said secondary interface such that at least a portion of a serial data message transmitted on said secondary bus is replaced by data stored in said data storage as said serial data message is communicated to said primary one wire bus.

6. (Canceled)

7. (Previously Amended) A method for inserting known data into a data stream between a master and a slave device bus including the steps of:

(a) providing a primary one-wire bus in electrical communication between the master and a translator;

(b) providing a secondary one-wire bus in electrical communication between the slave and said translator;

(c) waiting for a reset pulse on said primary one-wire bus;

(d) receiving a ROM command at said translator on said primary one-wire bus;

(e) determining if said ROM command is a read command, a match command, a search command, or a skip command;

(f) if said ROM command is a read command, performing the steps of:

(i) from said translator, transmitting predetermined data on said primary one-wire bus; and

(ii) returning to step (c)

(g) if said ROM command is a match command performing the steps of:

(i) at said translator, receiving an identifier on said primary one-wire bus;

(ii) comparing said received identifier to a first predetermined identifier; and

(iii) proceeding to step (j)

(h) if said ROM command is a search command performing the steps of:

(i) from said translator, transmitting the first bit of a second predetermined identifier having a plurality of bits on said primary one-wire bus;

(ii) from said translator, transmitting the complement of said first bit of said second predetermined identifier on said primary one-wire bus;

(iii) at said translator, receiving a bit on said primary one-wire bus; and

(iv) comparing said received bit to said first bit of said second predetermined identifier;

(v) repeating steps (h)(i) through (h)(iv) for each bit of said plurality of bits; and

(vi) proceeding to step (j);

(i) if said ROM command is a skip command proceeding to step (j);

(j) at said translator, receiving a memory command from said primary one-wire bus;

(k) at said translator, receiving a memory address from said primary one-wire bus;

(l) if said memory command is a read command performing the steps of:

(i) at said translator, receiving slave data on said secondary one-wire bus;

(ii) from said translator, transmitting said slave data on said primary one-wire bus;

(iii) repeating steps (l)(i) - (l)(ii) until a reset pulse is received on said primary one-wire bus;

(iii) returning to step (d);

(m) if said memory command is a write command, performing the steps of:

(i) at said translator, receiving slave data on said primary one-wire bus;

(ii) from said translator, transmitting said slave data on said secondary one-wire bus;

(iii) at said translator, receiving verification data on said secondary one-wire bus;

(iv) from said translator, transmitting said verification data on said primary one-wire bus;

(v) at said translator, receiving a write pulse on said primary one-wire bus;

(vi) from said translator, transmitting a write pulse on said secondary one-wire bus;

(vii) at said translator, receiving said slave data on said secondary one-wire bus;

(viii) from said translator, transmitting said slave data on said primary one-wire bus;

(ix) repeating steps (m)(i) - (m)(viii) until a reset pulse is received on said primary one-wire bus;

54 (x) returning to step (d).

8. (Canceled)